ABSTRACT OF THE DISCLOSURE

An integrated memory and method for testing an integrated memory is provided herein. In order to test an integrated memory having a main data memory (SP) with a plurality of data memory units, a data memory unit is addressed and input test data for testing the addressed data memory unit are applied to the main data memory (SP). The output test data are read out from the main data memory (SP) and compared with expected desired output test data in a self-test unit (STE). Deviations detected during the comparison are buffer-stored in a redundancy analysis memory (RAS). These information items buffer-stored in the redundancy analysis memory (RAS) are read out and transferred to a computing unit (RE). In the computing unit (RE), the defect positions in the output test data are identified, and a repair strategy is determined by means of redundant rows and/or redundant columns and/or redundant words provided. The redundant words required for the repair strategy are written to the redundancy analysis memory (RAS) and activated.